1)

Problem: Too many capacity misses in the data cache

Solution: Increase size of cache

Drawback: larger latency, power

Problem: Too many control hazards

Solution: dynamic branch prediction

Drawback: more power consumption

Problem: Our carry lookahead adder is too slow

Solution: use hierarchical adder, pipelining

Drawback: increase complexity

Problem: We want to be able to use a larger immediate field in the MIPS ISA

Solution: decrease registers, increase instruction size, decrease OP code

Drawback: resource spilling, complexity of coding will grow, decrease instruction

Problem: The execution time of our CPU with a single-cycle datapath is too high

Solution: multicycle, pipelining

Drawback: complexity (more hardware such as more latches), increase CPI